

HARI-0600

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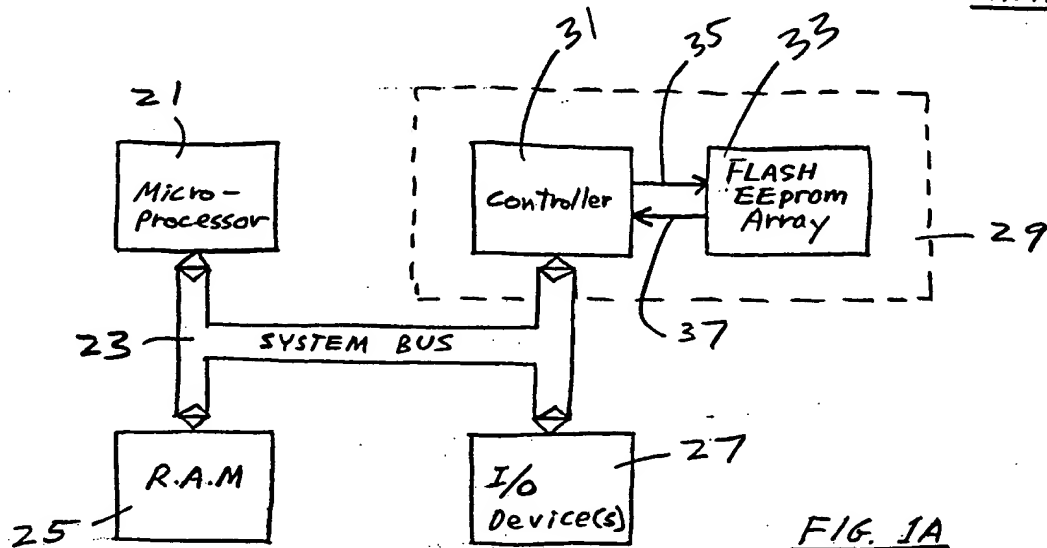


FIG. 1A

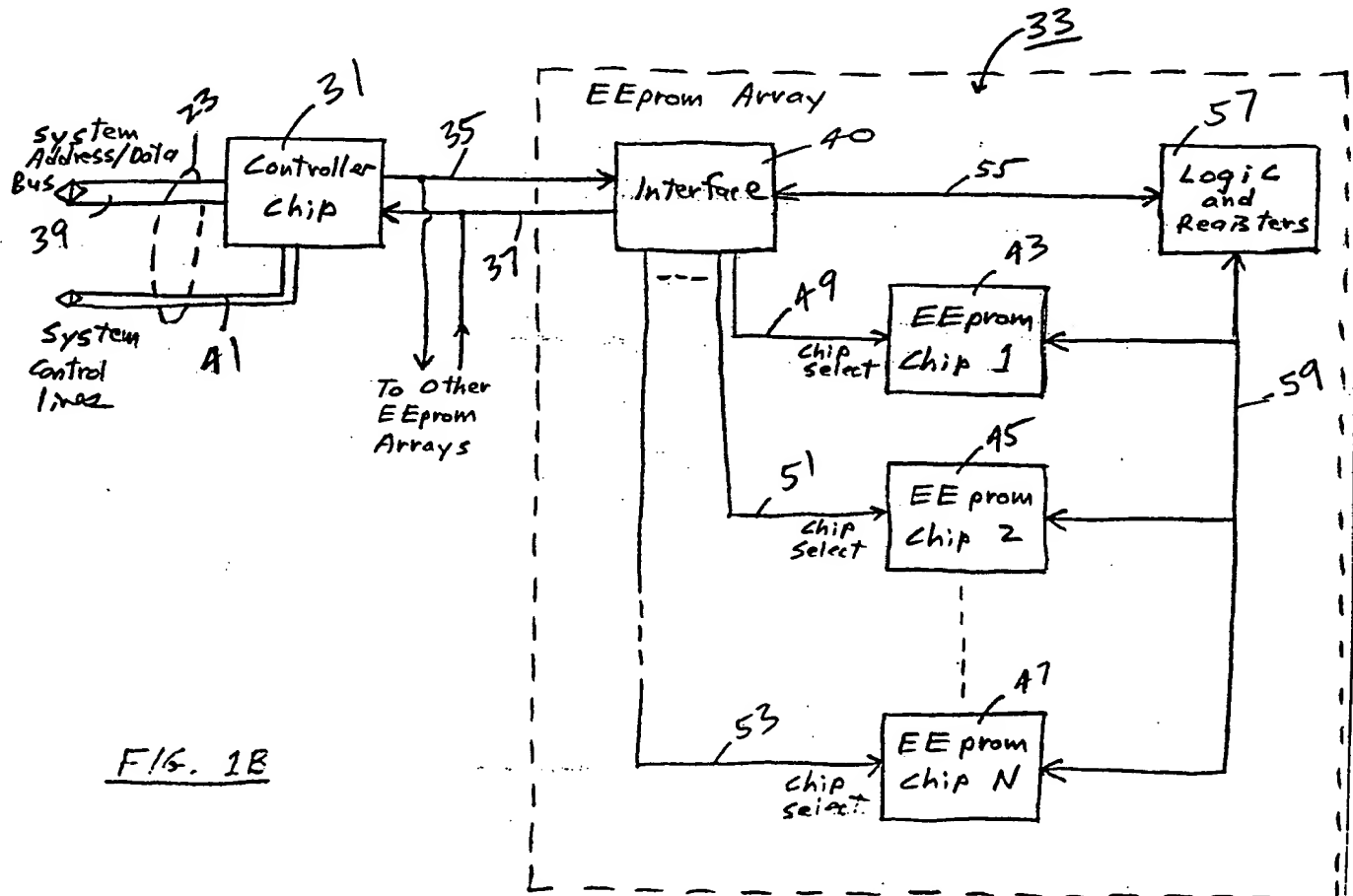


FIG. 1B



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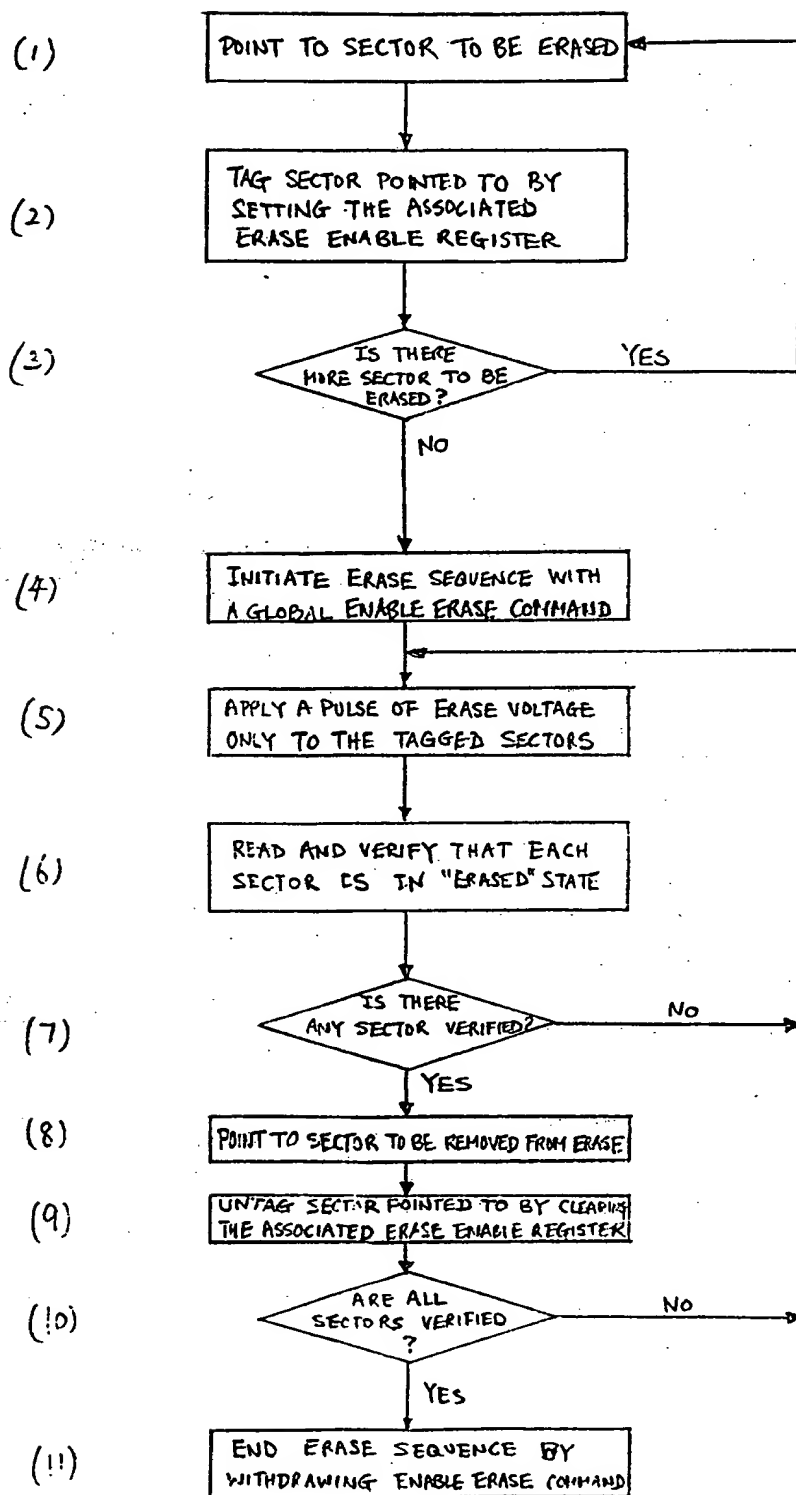
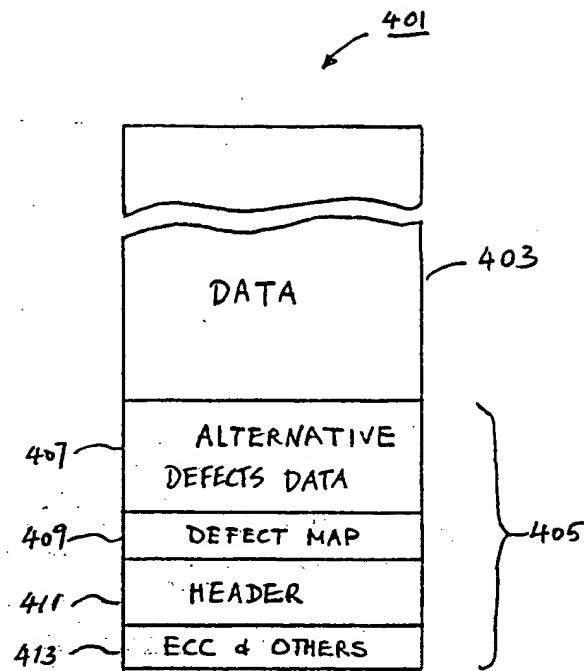


FIG - 4



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SECTOR PARTITION

FIG-5

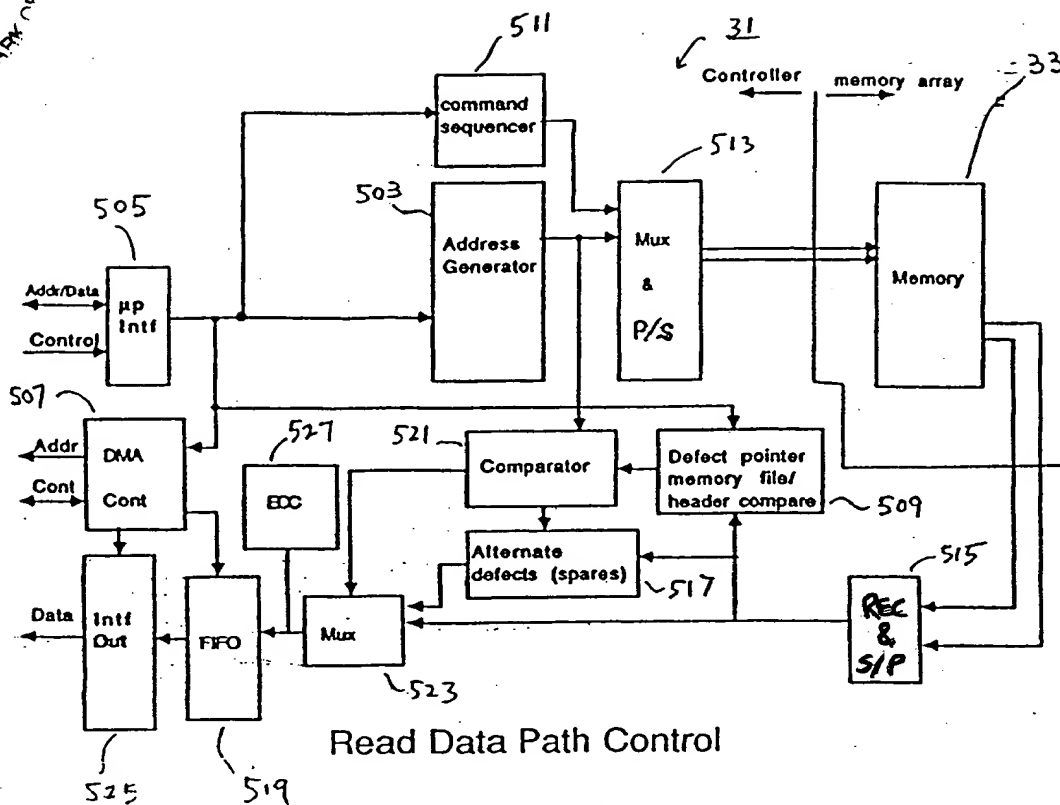


FIG. 6

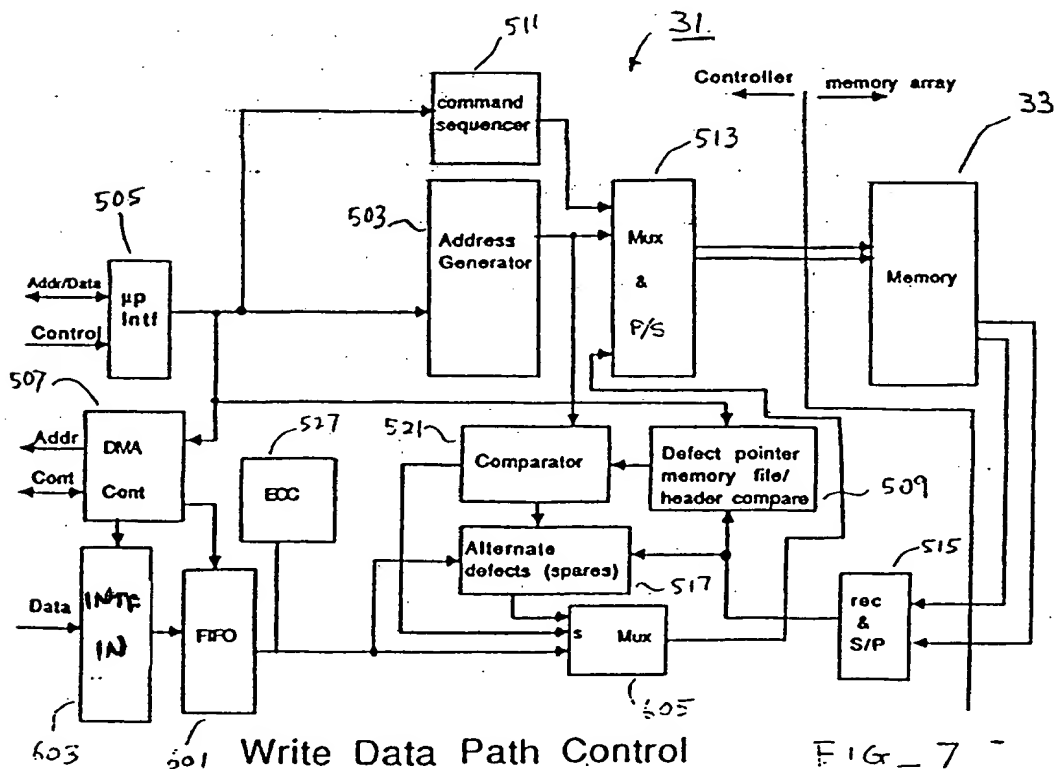


FIG. 7

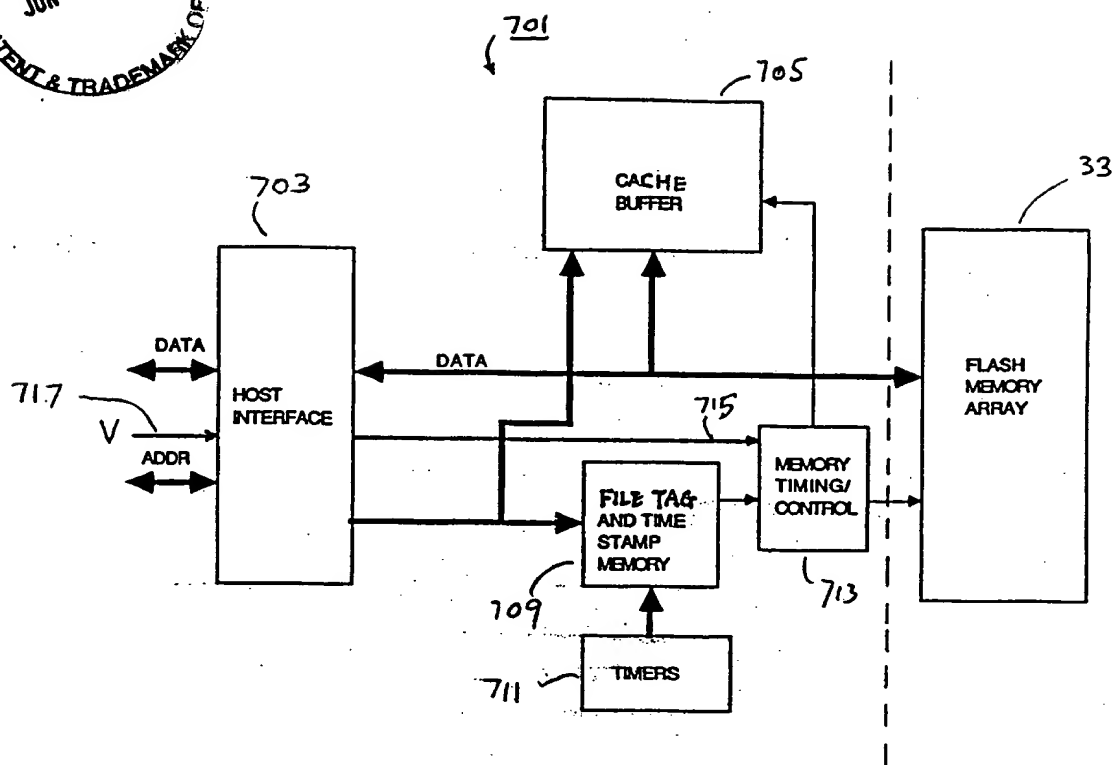


FIG. 8

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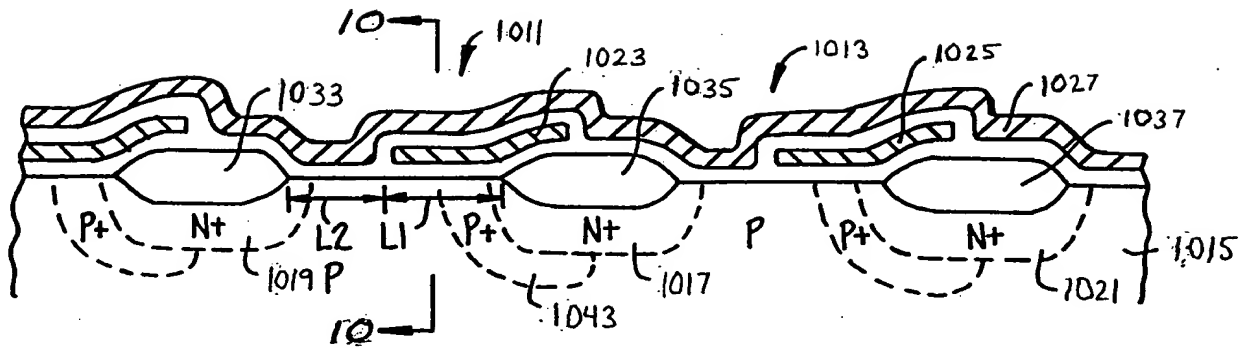


FIG. 9

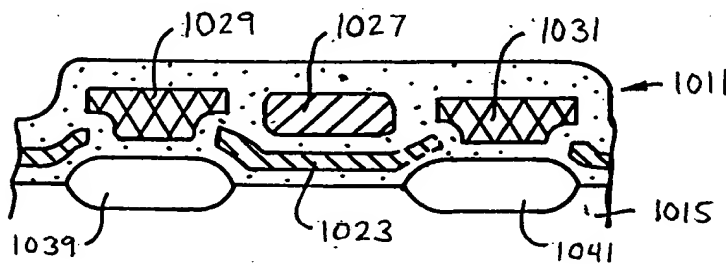


FIG. 10

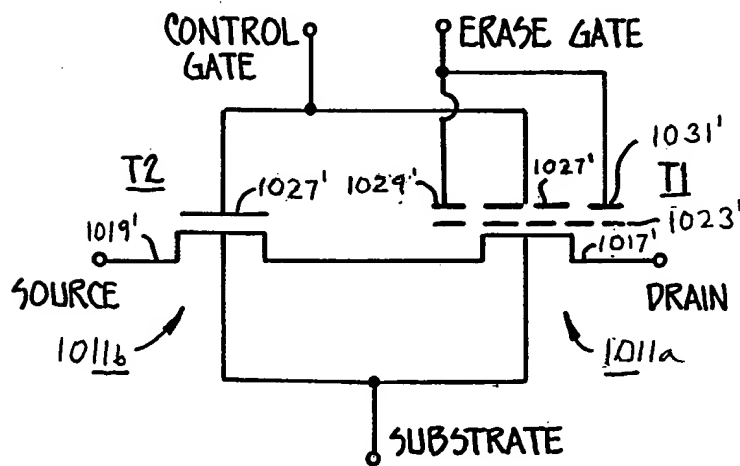


FIG. 11



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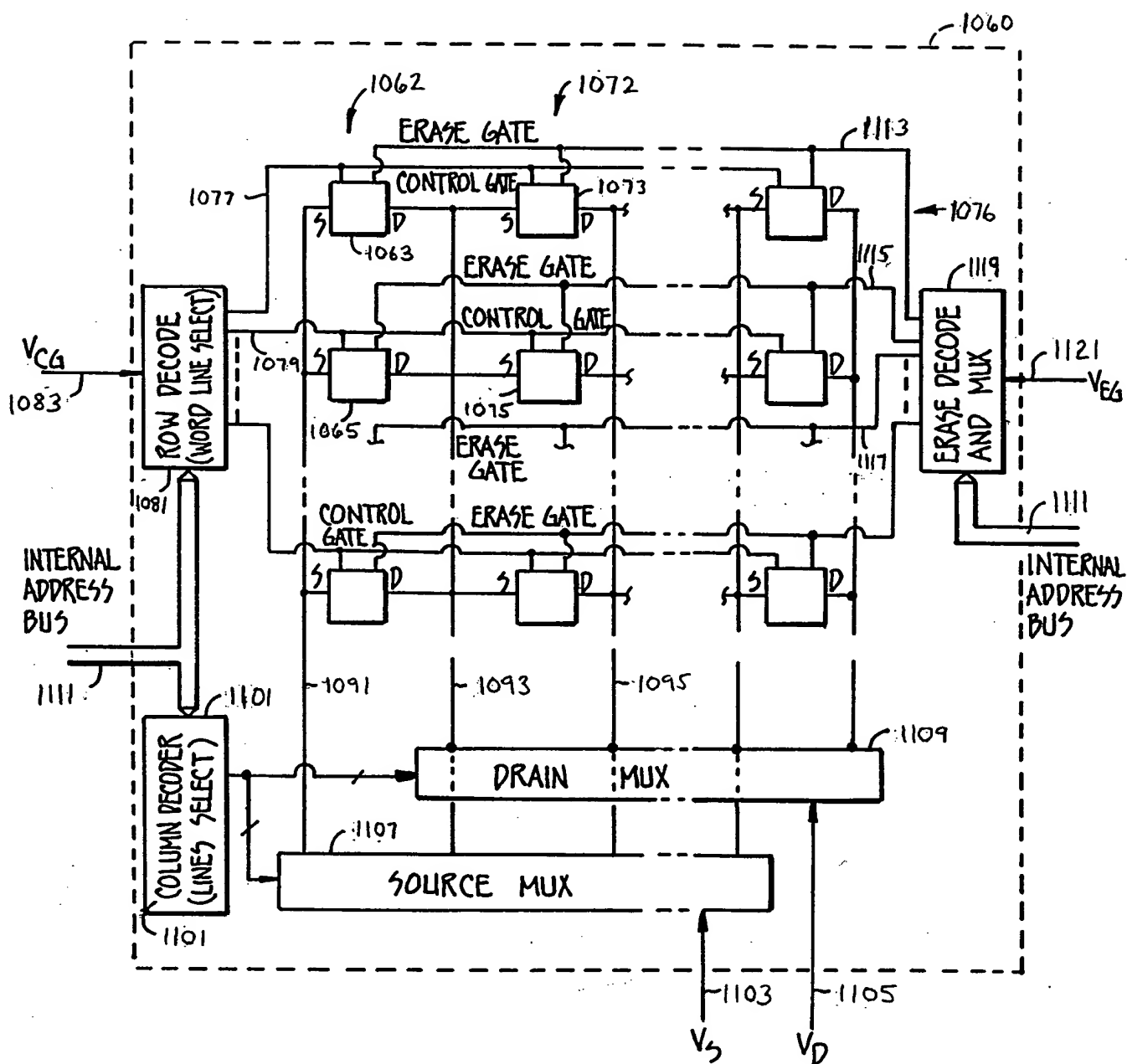


FIG. 12.

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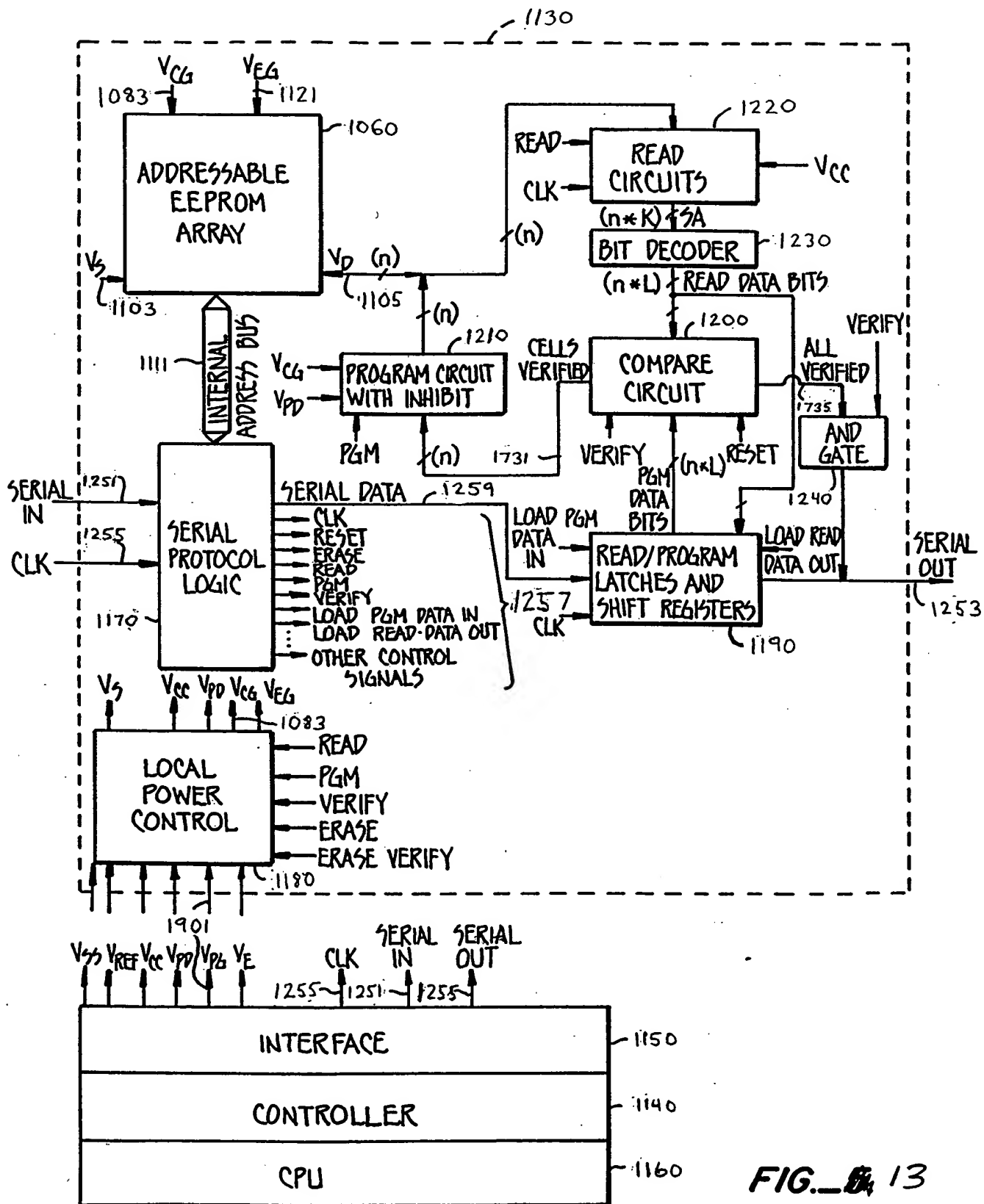


FIG. 13

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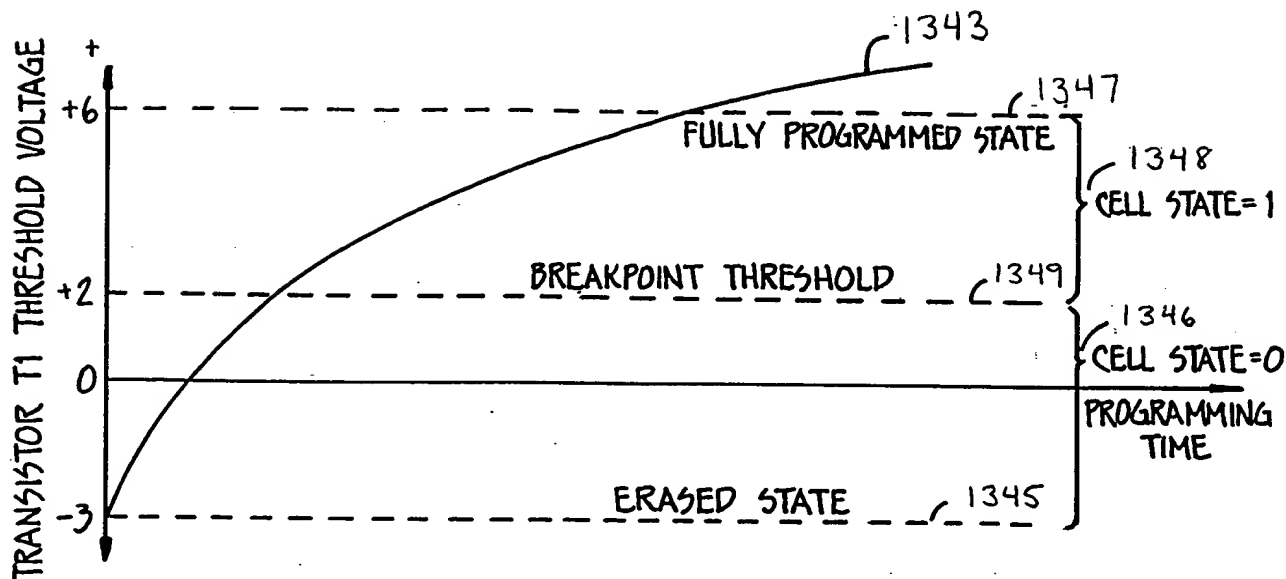


FIG. 14.

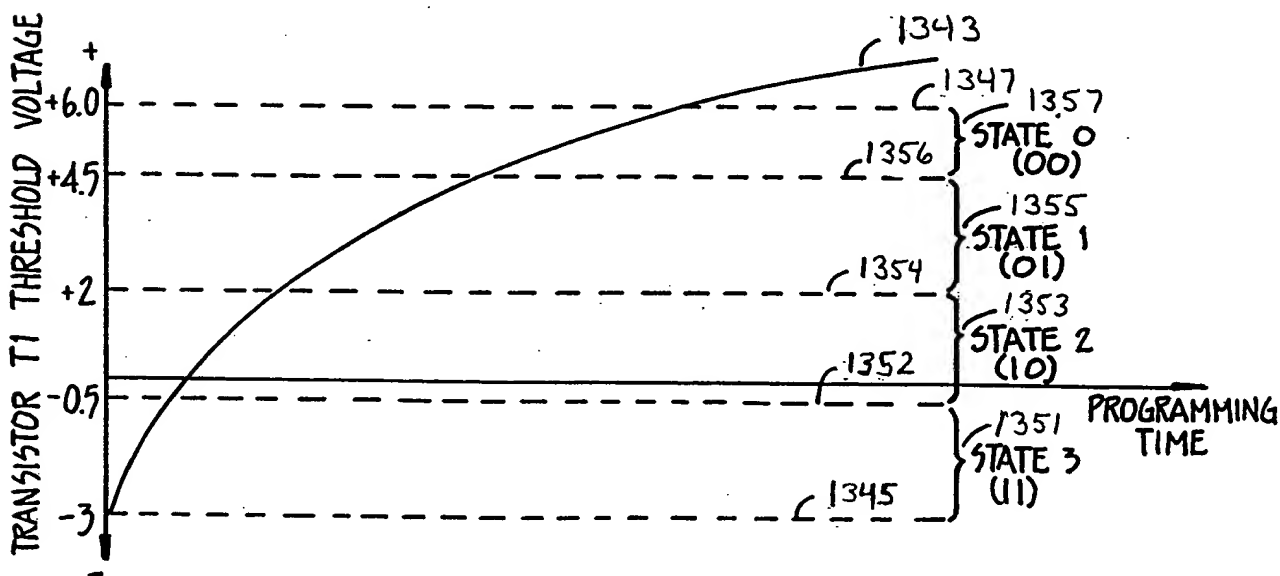


FIG. 15A

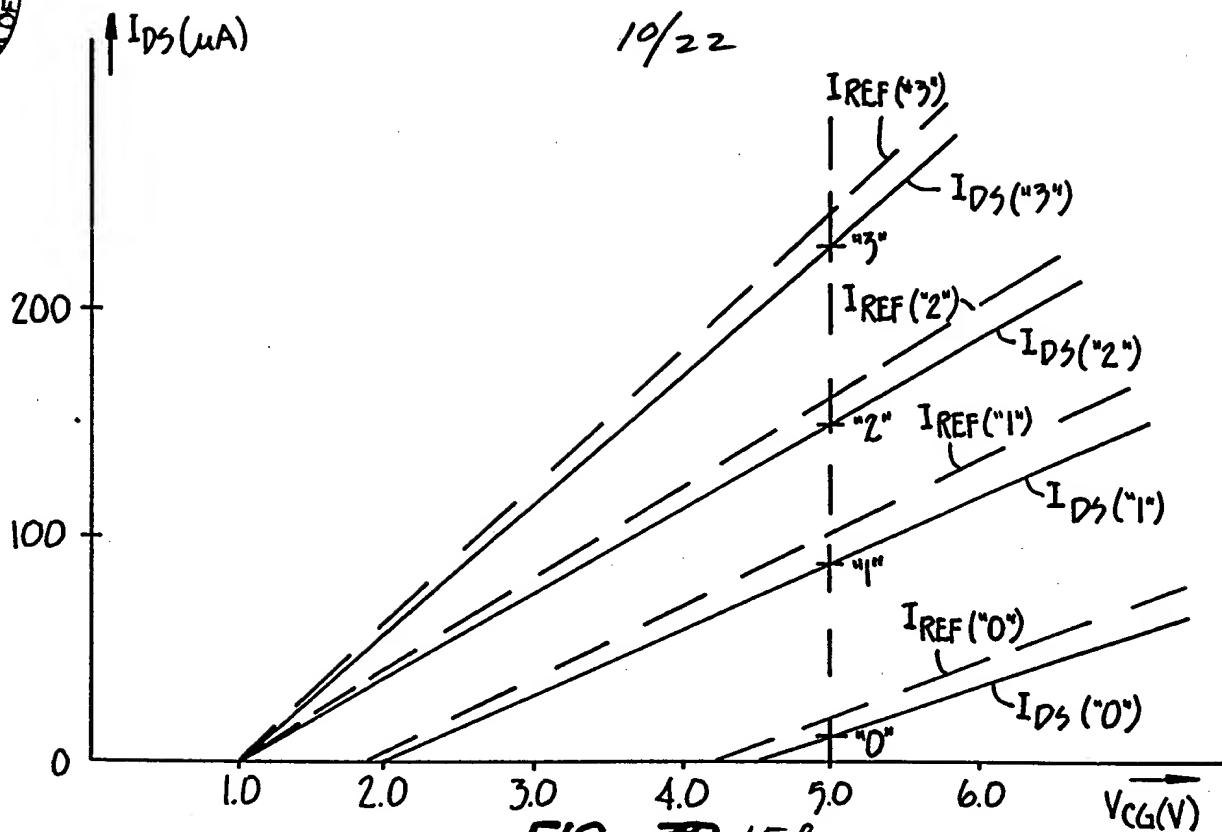


FIG. 15B

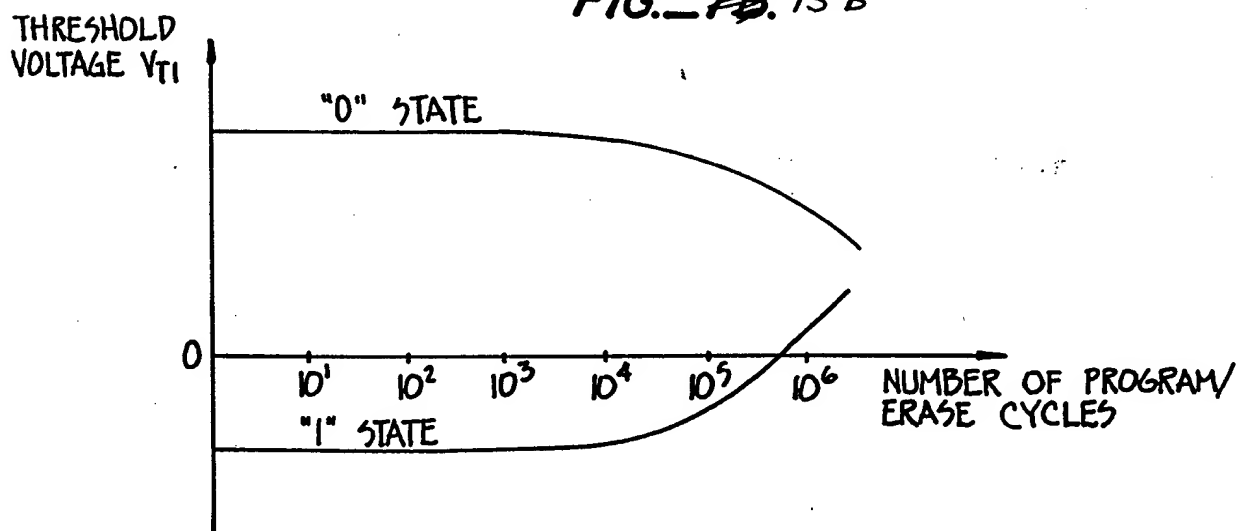


FIG. 16A

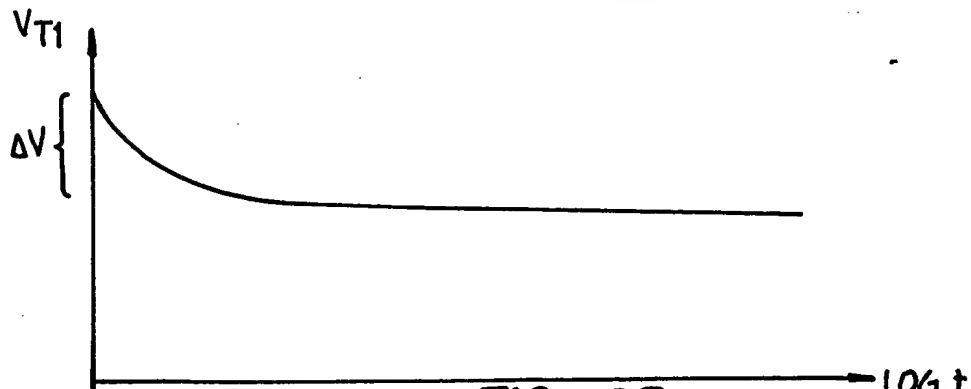


FIG. 16B

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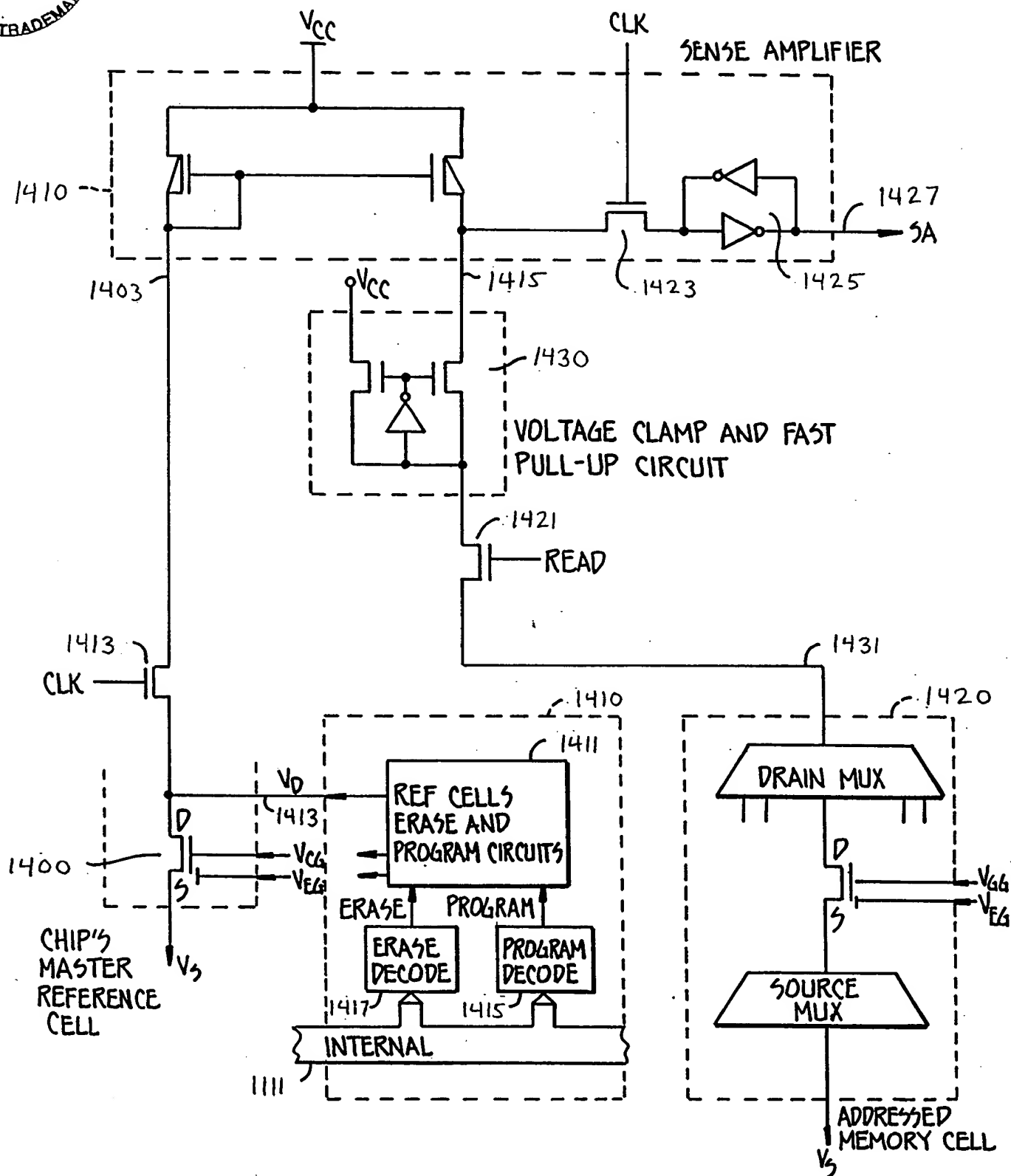


FIG. 17A

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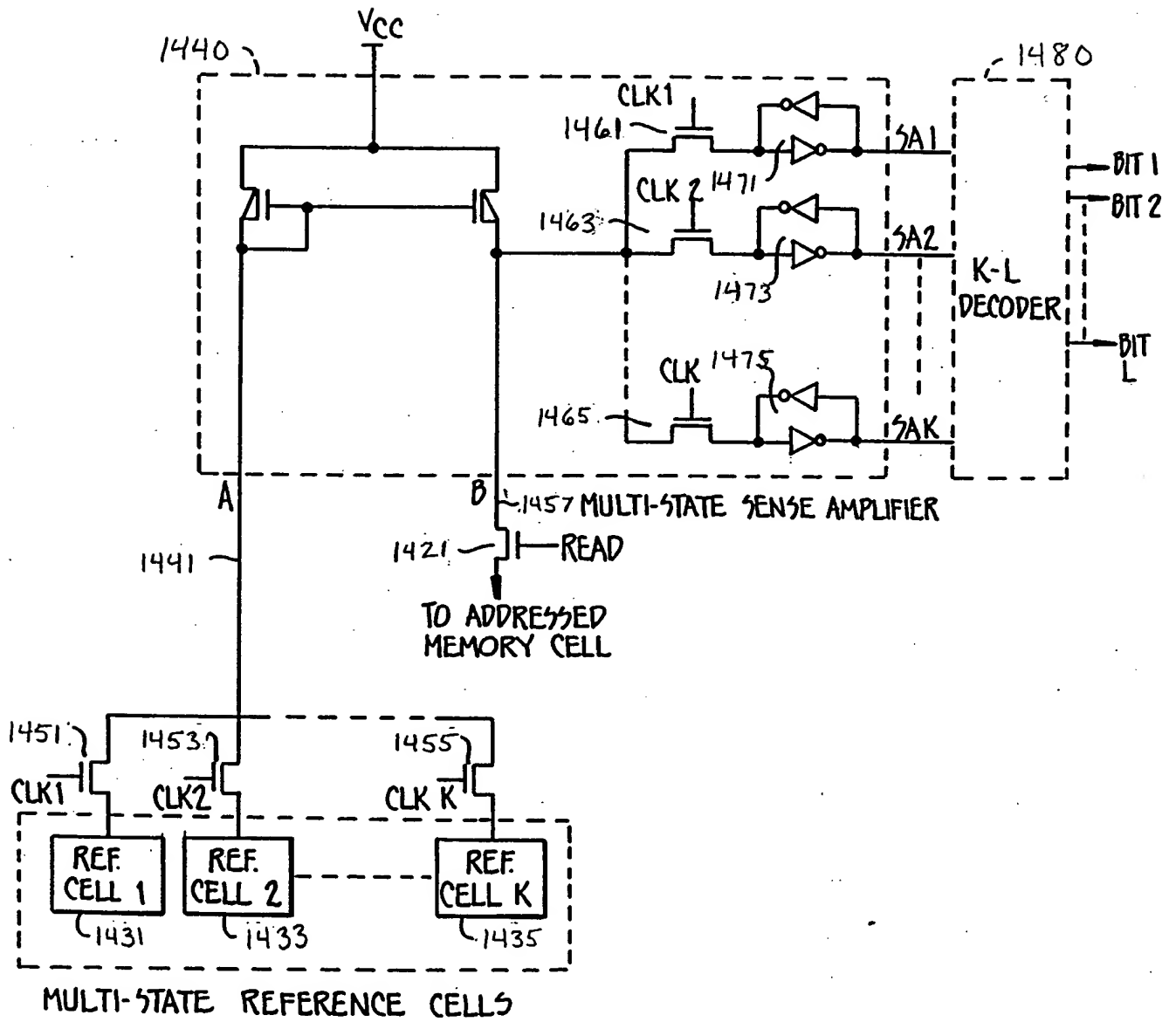
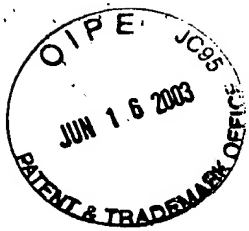


FIG. 17B



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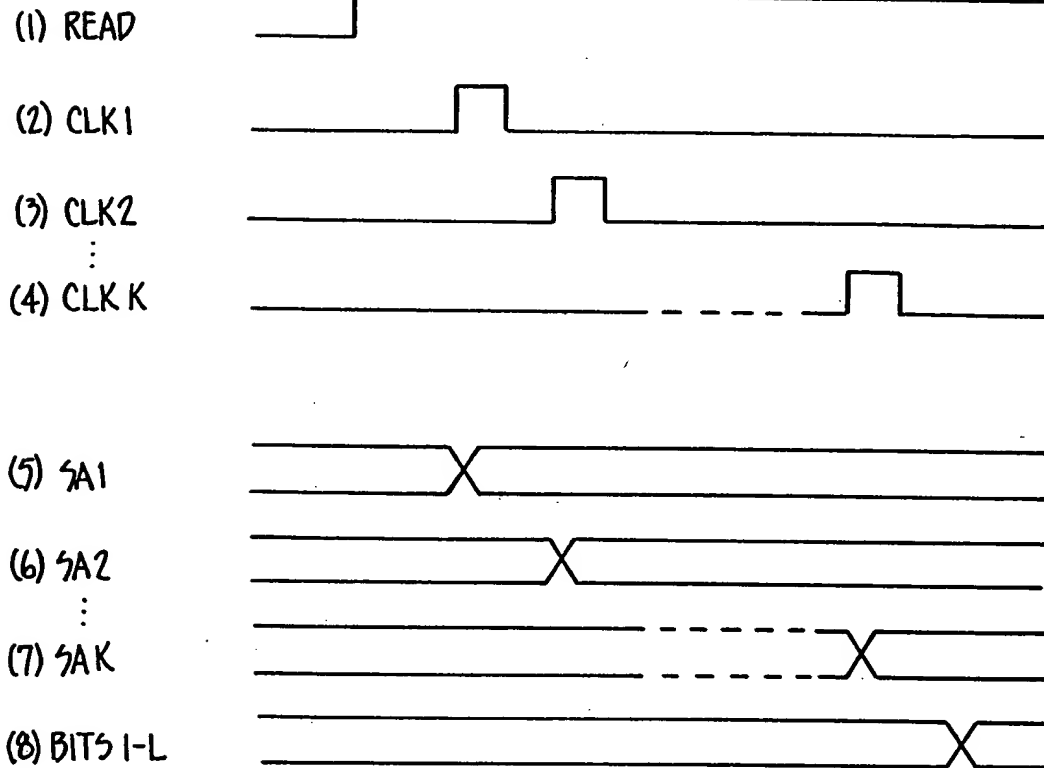


FIG. ~~17A~~ 17C

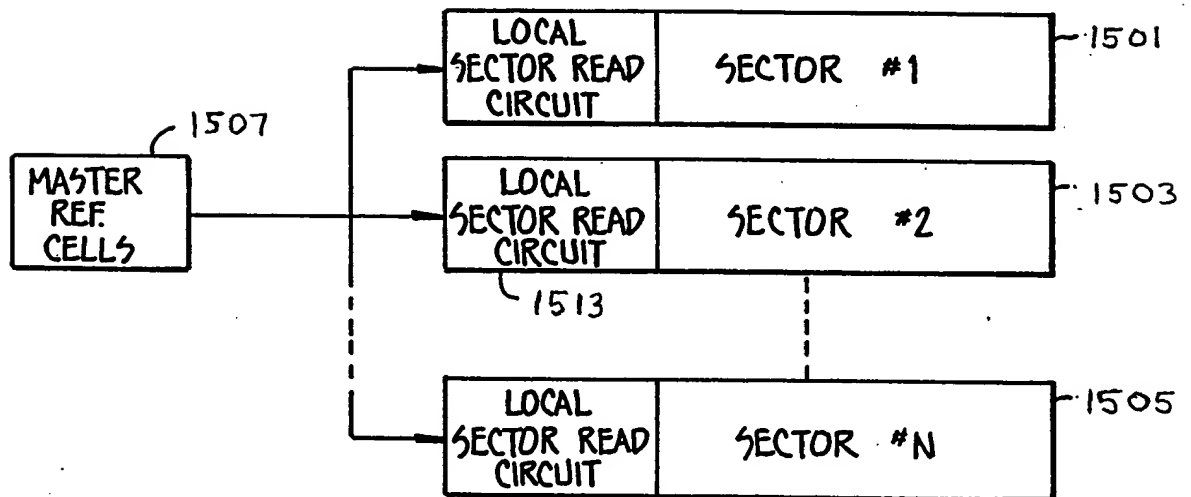
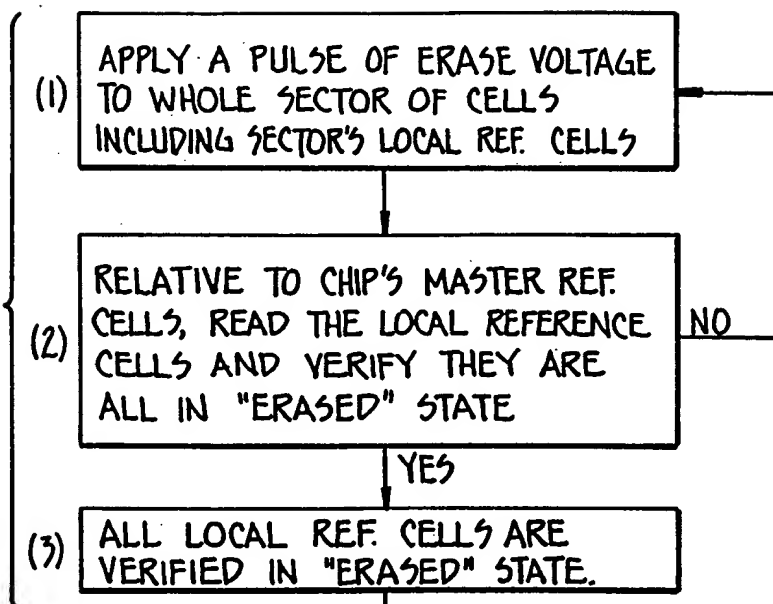


FIG. ~~18A~~ 18



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SECTOR LOCAL
REF. CELLS ERASE
AND VERIFY
ALGORITHM



SECTOR'S LOCAL
REF. CELLS
PROGRAM AND
VERIFY ALGORITHM

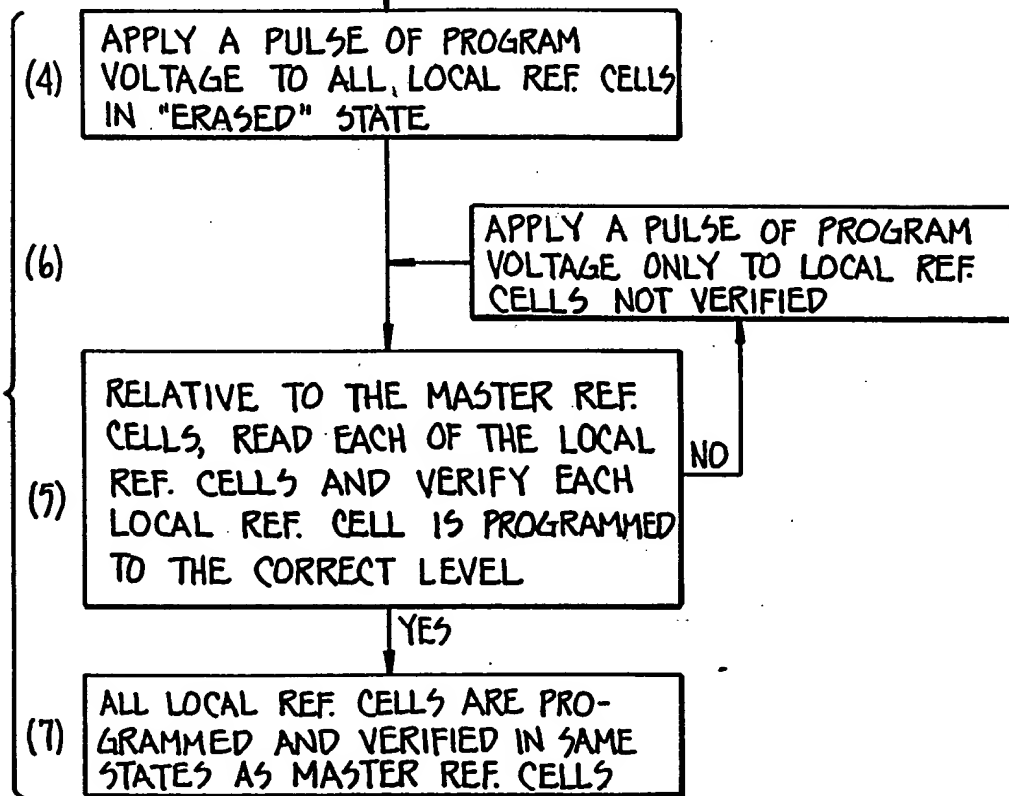


FIG. 19

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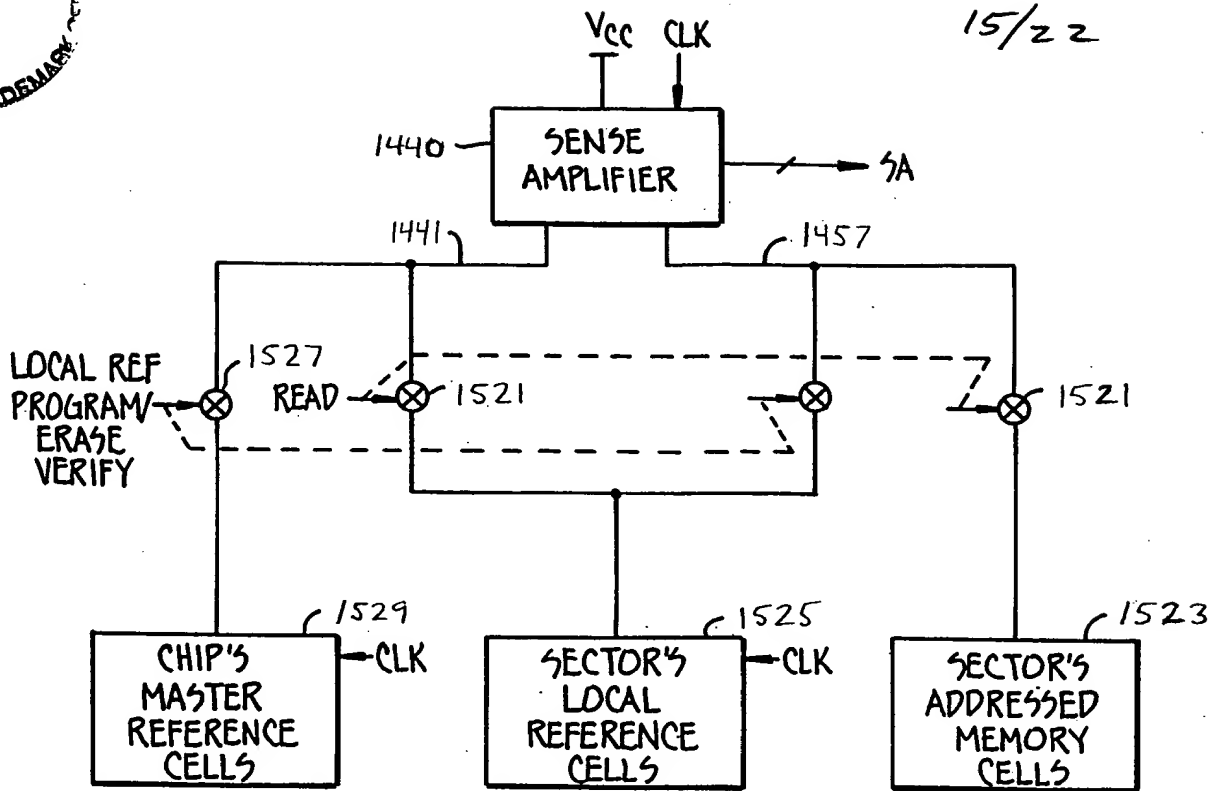


FIG. 12A 20A

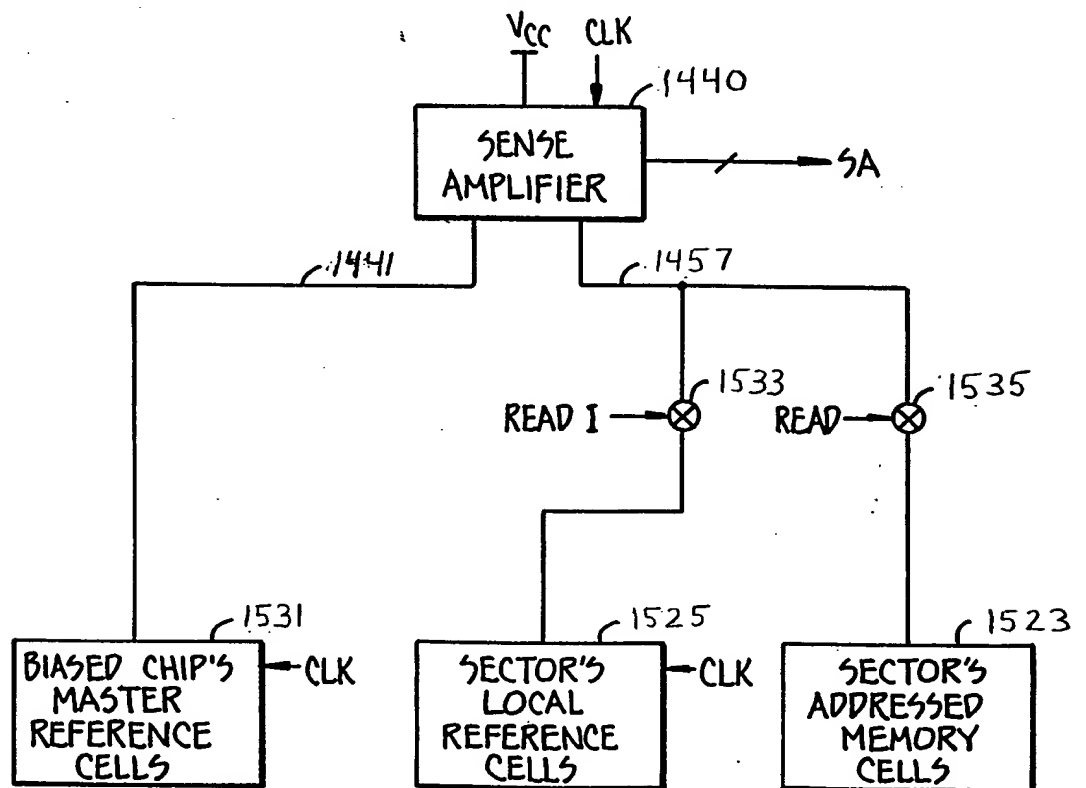


FIG. 13A 21A

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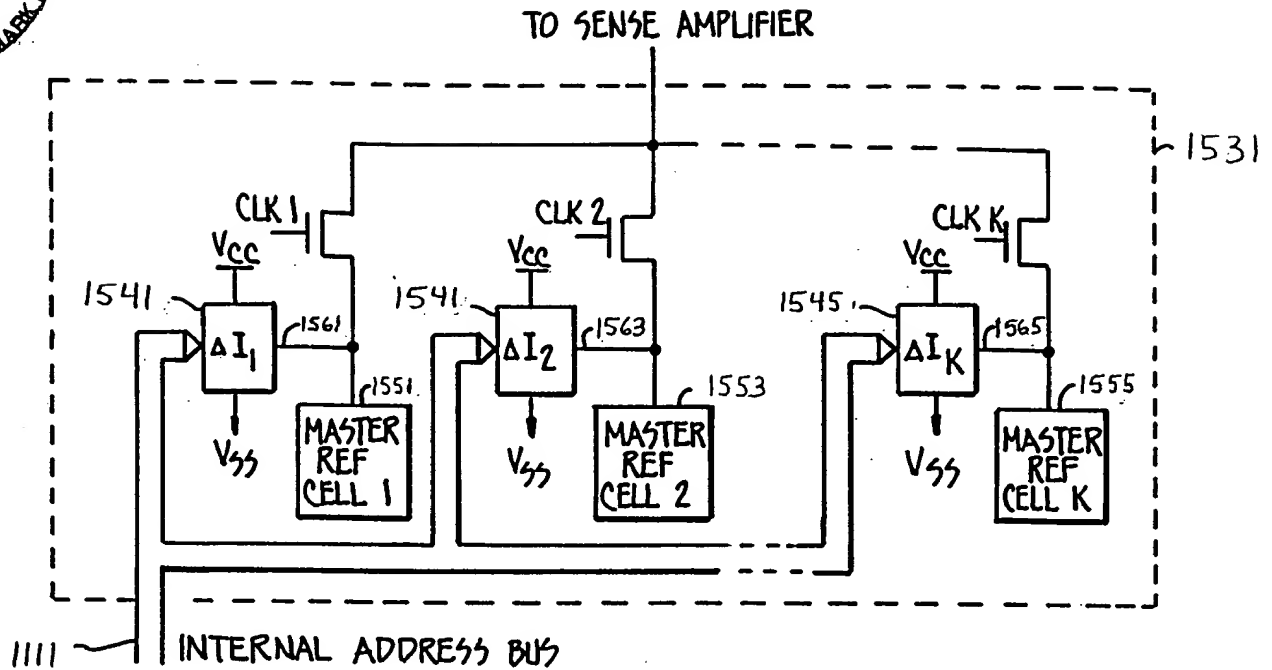


FIG. ~~21B~~ 21B

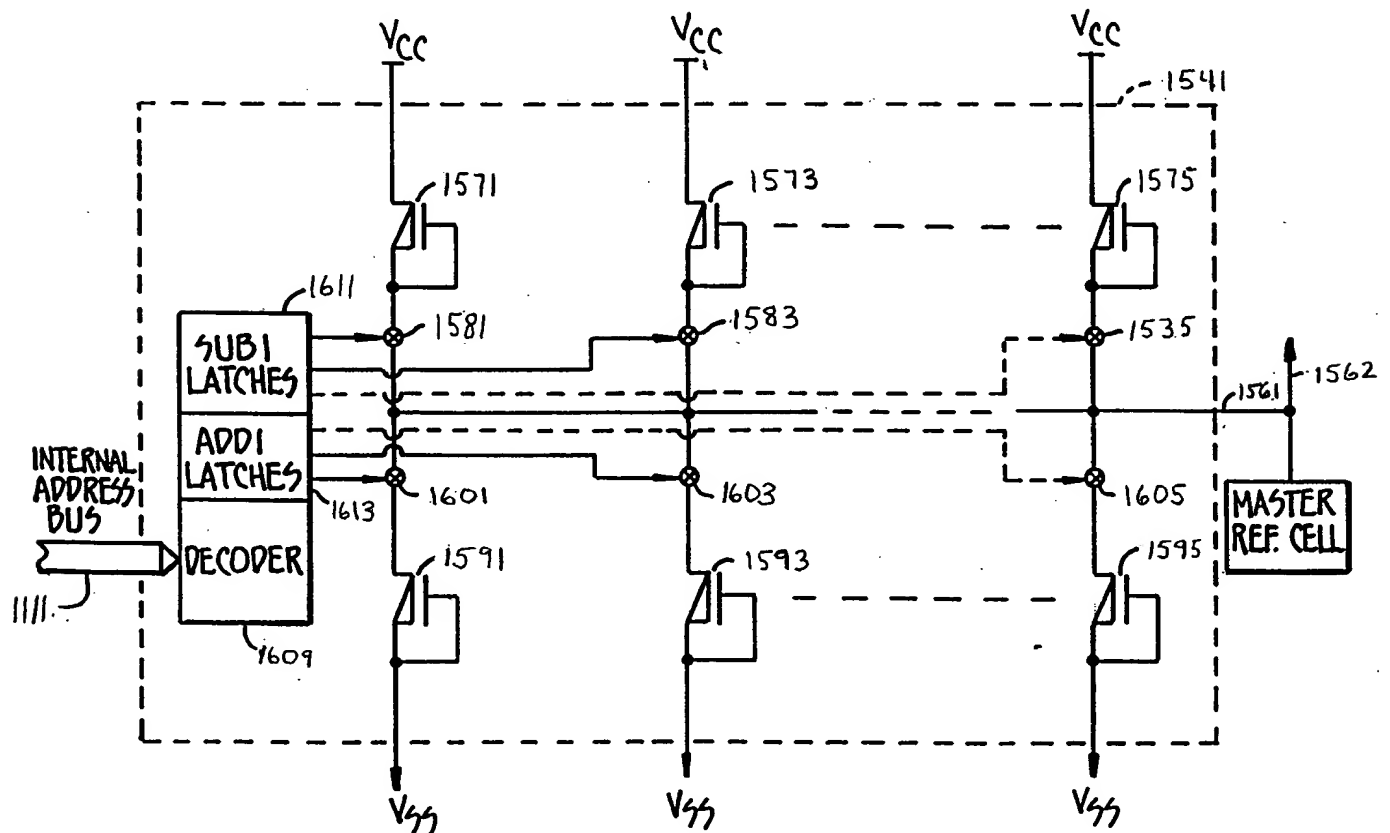


FIG. ~~21C~~ 21C



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LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED
AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

RELATIVE TO THE LOCAL REF. CELLS,
READ THE ADDRESSED CELLS

FIG. ~~12B~~, 20B

(1)

LOCAL REF. CELLS ARE PREVIOUSLY
PROGRAMMED AND VERIFIED IN SAME
STATES AS MASTER REF. CELLS

(2)

RELATIVE TO THE LOCAL REFERENCE
CELLS READ THE MASTER REF. CELLS

(3)

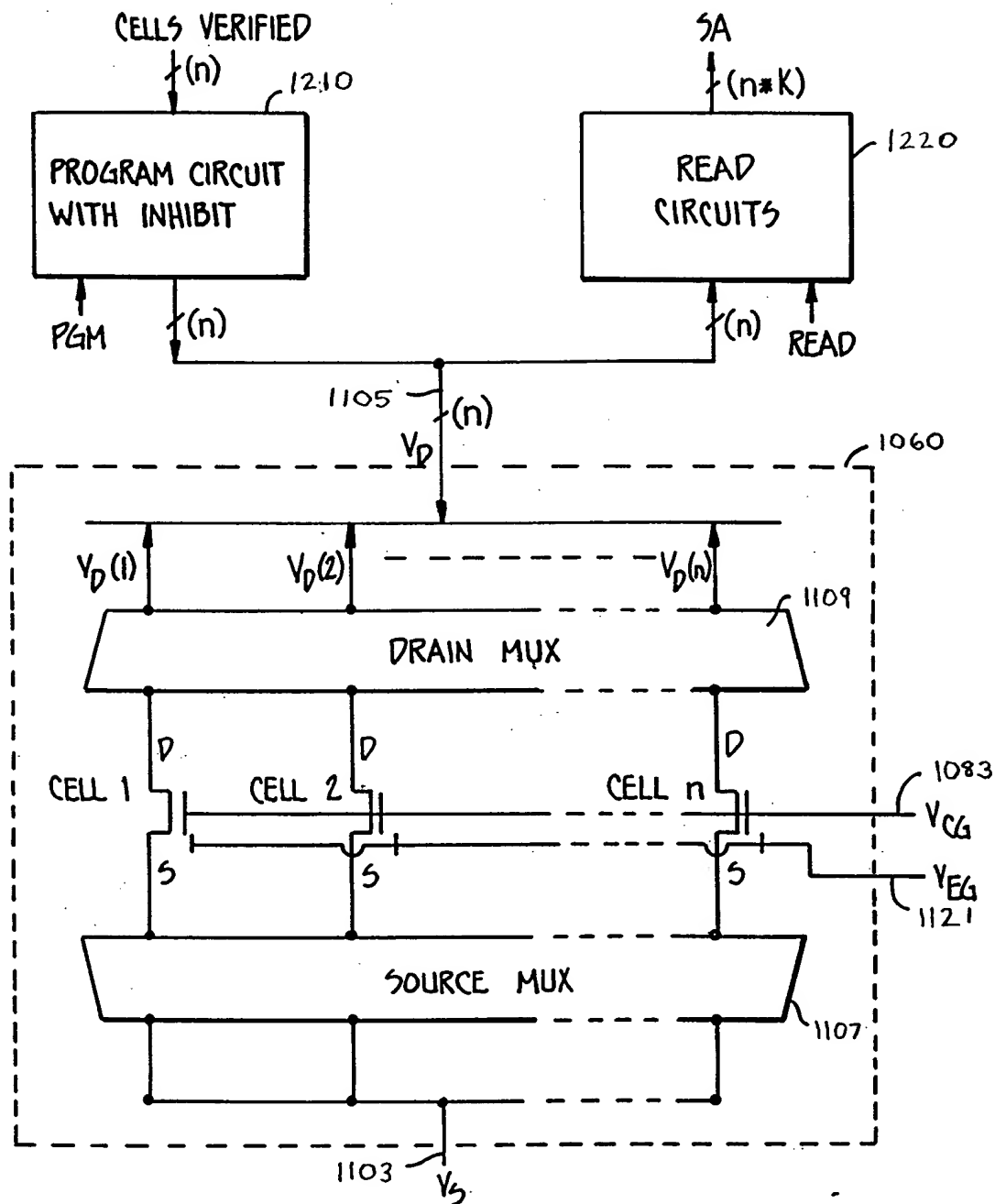
DETERMINE THE DIFFERENCES, IF ANY
AND BIAS. THE MASTER REF CELLS'
CURRENTS SUCH THAT THE SAME
READING IS OBTAINED RELATIVE TO
THE BIASED MASTER REF. CELLS
AS RELATIVE TO THE LOCAL
REF. CELLS

(4)

RELATIVE TO THE BIASED MASTER
REF. CELLS, READ THE ADDRESSED CELLS

FIG. ~~13D~~, 21D

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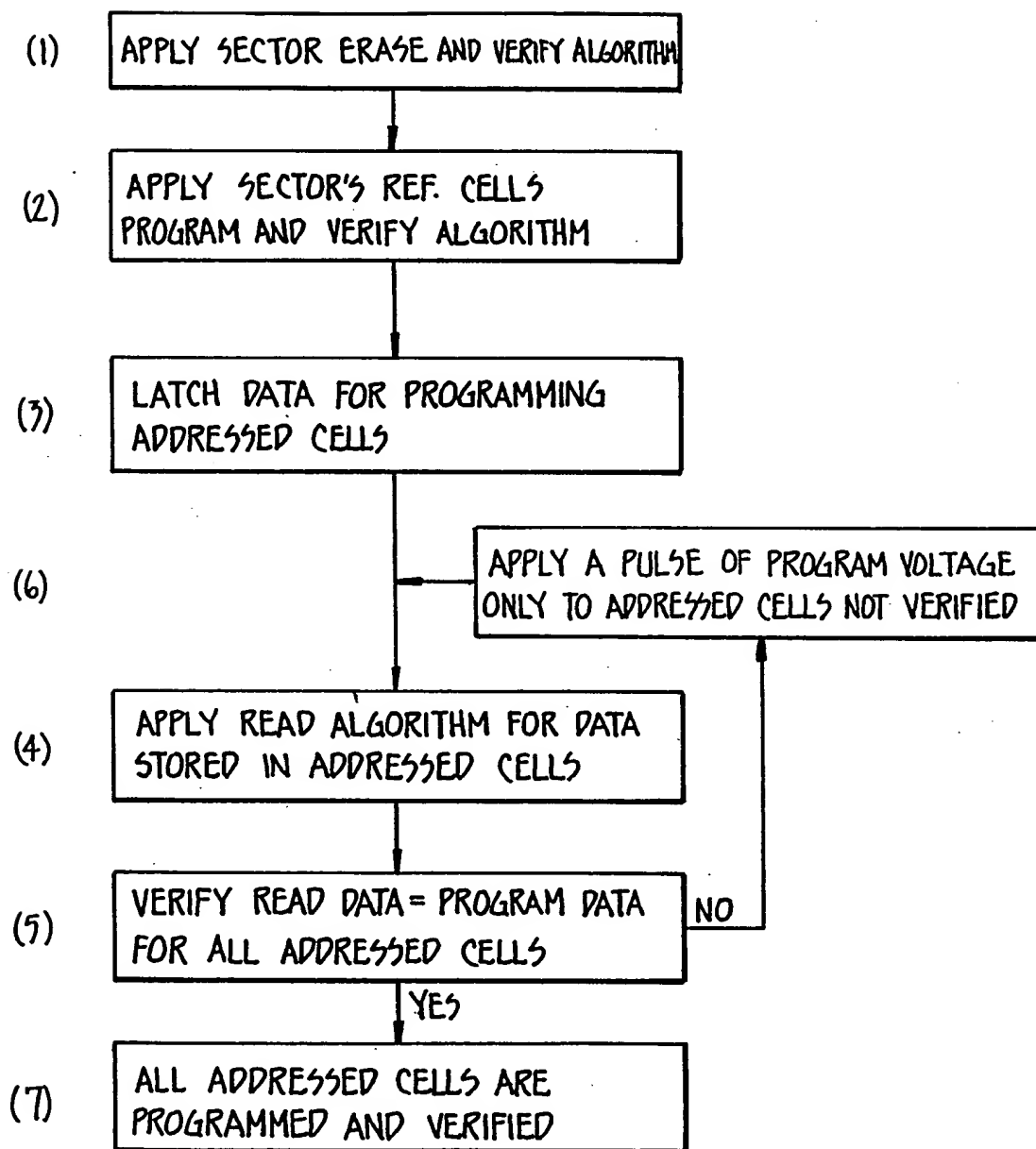


READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.



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PROGRAM ALGORITHM

FIG. 23



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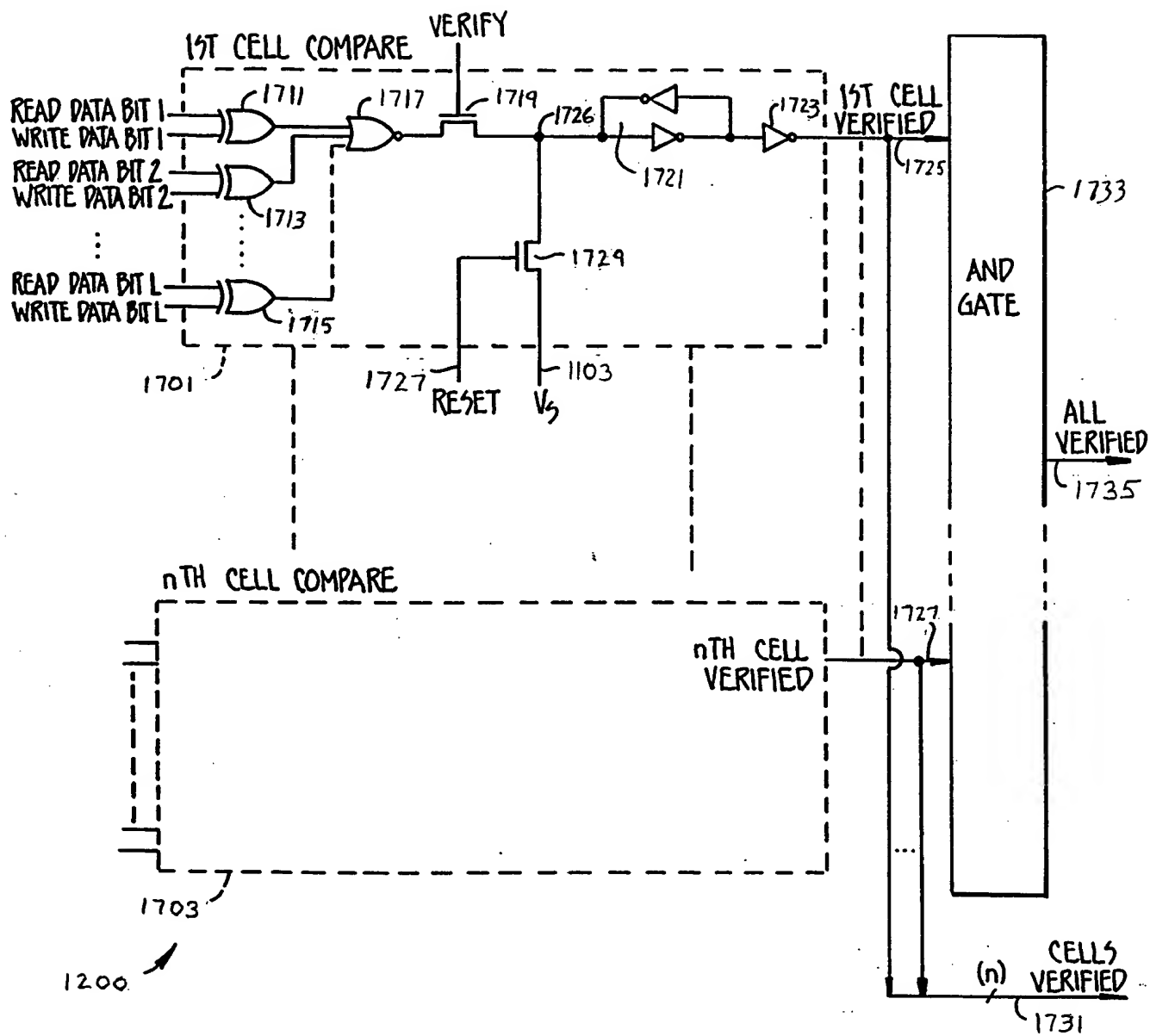


FIG. 24

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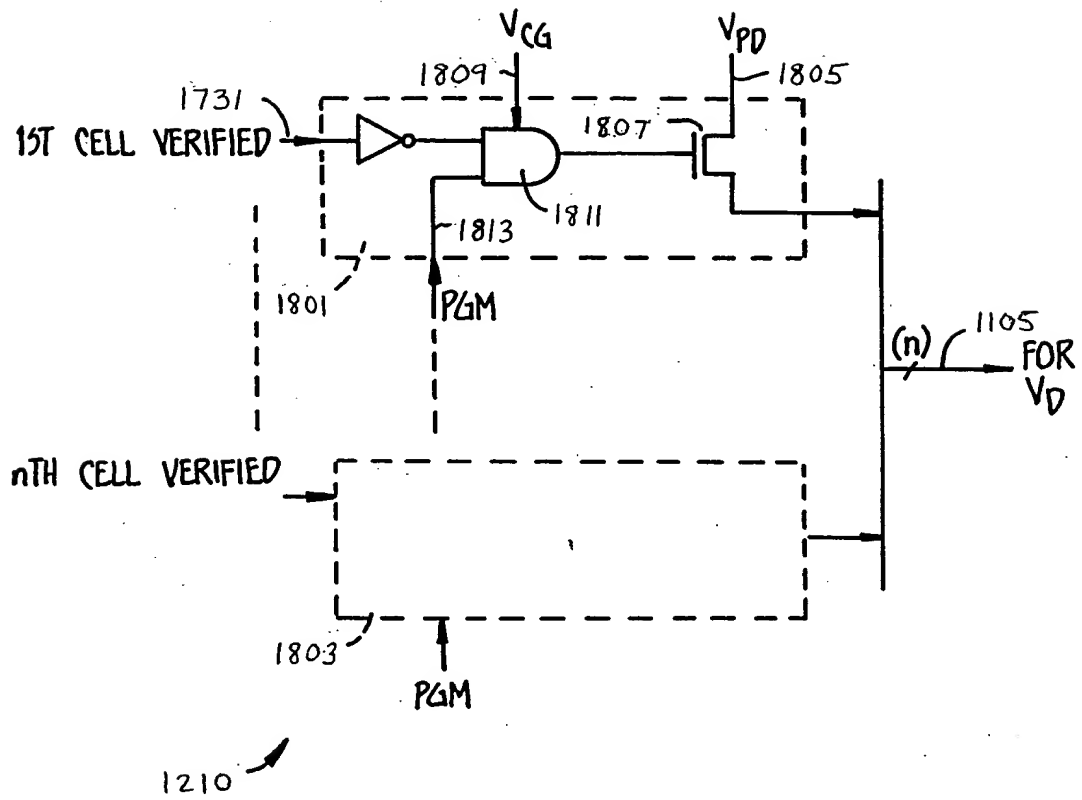


FIG. 25



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	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC} + \delta V$	V_{CC}	$V_{CC} - \delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$V_{SS}=0V$, $V_{REF}=1.5V$, $\delta V=0.5V - 1V$

~~TABLE 2~~ FIG. 27